UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,475	09/17/2003	Steven Towle	Intel/16652	4376

34431 7590 04/09/2007

HANLEY, FLIGHT & ZIMMERMAN, LLC
150 S. WACKER DRIVE
SUITE 2100
CHICAGO, IL 60606

EXAMINER	
NGUYEN, CUONG QUANG	
ART UNIT	PAPER NUMBER
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/664,475	TOWLE ET AL.	
	Examiner	Art Unit	
	Cuong Q. Nguyen	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) 25 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 01-20-04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Species I, claims 1-24 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, and 11-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Kimerling (US 2003/0091264).

Regarding claims 1, 2, Kimerling discloses an apparatus comprising: a substrate; a waveguide (16) mounted on the substrate; and an optoelectric chip (6) (a flip-chip)

bonded to the substrate and having an optical element (Ge detector 12) directly engaging the waveguide. See Fig.1.

Regarding claim 3, Kimerling teaches that the optical element comprises a transceiver, a receiver or a transmitter. See [0016] , [0018], [0020] and claim 1.

Regarding claim 4, as shown in Kimerling Fig.1, the optoelectronic chip is bonded to the substrate via an electrical connection (solder bump 26) between facing surfaces of the optoelectronic chip and substrate.

Regarding claims 11 and 12, as shown in Kimerling Fig.1, the waveguide is inherently to have a thermal stability sufficient to withstand a flip-chip bonding temperature and a glass transition temperature in order to operate properly.

Regarding claims 19, 20, as shown in Kimerling Fig.1. the combined thickness of solder bumps is appropriately equal to the height of the waveguide.

Regarding claim 21, the waveguide is inherently to have a glass transition temperature above the melting point of the solder bump in order to operate properly.

Regarding claim 22, as shown in Kimerling Fig.1, the substrate including a FCPGA substrate.

Claims 1-8, and 10-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Towle et al. (US 6,).

Regarding claims 1, 2, Towle et al. discloses an apparatus comprising: a substrate; a waveguide (112) mounted on the substrate; and an optoelectric chip (114) (a flip-chip) bonded to the substrate and having an optical element (116) directly engaging the waveguide. See Fig.3.

Regarding claim 3, Towle et al. teaches that the optical element comprises a transceiver, a receiver or a transmitter. See col.3 lines 43-50.

Regarding claim 4, as shown in Towle et al.'s Fig.3, the optoelectronic chip is bonded to the substrate via an electrical connection (solder bump 215) between facing surfaces of the optoelectronic chip and substrate.

Regarding claim 5 and 6, as shown in Towle et al.'s Fig.3, an underfill material between the optoelectronic chip and the substrate, wherein the underfill material is not formed between the waveguide and optoelectronic chip.

Regarding claims 7 and 8, as shown in Towle et al.'s Fig.3, the waveguide including a metallized mirror (136).

Regarding claim 10, Towle et al. teaches that the waveguide including a planar waveguide. See col.3 lines 20-25.

Regarding claims 11, 12,the waveguide is inherently to have a thermal stability sufficient to withstand a flip-chip bonding temperature in order to operate properly.

Regarding claims 19, 20, as shown in Towle et al. Fig.3, the combined thickness of solder bumps is appropriately equal to the height of the waveguide.

Regarding claim 21, the waveguide is inherently to have a glass transition temperature above the melting point of the solder bump in order to operate properly.

Regarding claim 22, as shown Towle et al.'s Fig.3, the substrate including a FCPGA substrate.

Claims 1-3, 7, 9-10, and 23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Kitamura et al. (US 2002/0135543).

Regarding claims 1, 2, Kitamura et al. discloses an apparatus comprising: a substrate (10); a waveguide (30) mounted on the substrate; and an optoelectric chip (50) (a flip-chip) [0049] bonded to the substrate and having an optical element (23) directly engaging the waveguide. See Fig.2.

Regarding claim 3, Kitamura et al. teaches that the optical element (light emitting element) comprises a transmitter.

Regarding claim 7, as shown in Kitamura et al.'s Fig., the waveguide including a mirror (30C).

Regarding claims 9 and 10, Kitamura et al. teaches that the waveguide is a planar waveguide or a volum diffraction grating. See [0048].

Regarding claims 23 and 24, as shown in Kitamura et al.'s Fig.2, the active waveguide is between passive waveguides which located to maintain a predetermined separation between the flip-chip (50) and the substrate (10), wherein the active waveguide and passive waveguide are separate waveguides.

The limitation "the first and second plurality of solder bumps having a combined thickness prior to solder which is greater than a height of the waveguide" in claim 19 and limitations in claims 13-18 are taken to be a product by process limitations, it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimerling in view of Yunus (US 6,907,151).

Regarding claim 5, Kimerling et al. does not explicitly teach that an underfill material disposed between the optoelectronic chip and the substrate.

It is conventional and also taght by Yunus that underfill material is commonly formed between the optoelectronic chip and the substrate.

It would have been obvious to one of ordinary skill in the art to form an underfill material between the optoelectronic chip and the substrate as taught by Yunus in order mitigate stresses on the silder joints arising from mismatches in thermal expansion between the optoelectronic chip and the substrate., See Yunus's col.4 lines 17-25.

Regarding claim 6, as shown in Kimerling Fig.1, it is no gap between the waveguide (16) and the Ge detector element (12). So, the underfill material would not be formed between the Ge detector element and the waveguide.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura et al.

Kitamura et al. does not explicitly teach that the mirror is a metallized mirror.

It is known and conventional that mirror of a waveguide is commonly being formed by metal because metal having good reflecting property.

So, it would have been obvious to one of ordinary skill in the art to form the mirror of metal.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong Nguyen whose telephone number is (571) 272-1661. The examiner can normally be reached on 8:00 am to 5:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

5. Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cuong Nguyen

Primary examiner

3/31/07